SON-1531

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of)
)
Yoshikazu KUROSE)
) Group Art Unit: 2671
Serial No. 09/283,231)
) Examiner: M. PADMANABHAN
Filed: April 1, 1999)
)
For: IMAGE PROCESSING APPARATUS)
AND METHOD OF PROCESSING)
IMAGES THAT STOPS OPERATION OF)
PIXEL PROCESSING CIRCUITS WHEN)
PIXEL DATA TO BE PROCESSED IS)
NOT NEEDED)

APPEAL BRIEF

Assistant Commissioner for Patents
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Sir:

This Appellant's Brief on Appeal is timely filed under the provisions of 37 CFR § 1.192 together with a Notice of Appeal filed concurrently herewith. By this brief, the authorities and arguments on which the Appellant will rely to maintain this appeal are set forth. The brief contains the items specified by Rule 192(c), under appropriate headings and in the requisite order.

I. REAL PARTY OF INTEREST

The real party of interest in this appeal is Sony Corporation of Tokyo, Japan

which is, by assignment of the inventor, the current owner of this patent application. The assignment was recorded on June 25, 1999, at Reel 010056 and Frame 0692.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to this application at this time.

III. STATUS OF THE CLAIMS

Claims 1 to 40 remain pending in this application, with all of the claims being rejected. The final rejections of claims 1 to 40 are the subject of this appeal.

A copy of the claims under final rejection (i.e., claims 1 to 40) is provided in the attached Appendix of Claims.

IV. STATUS OF THE AMENDMENTS

An Amendment was filed on October 17, 2001, in response to the initial Office Action of July 31, 2001. The changes included in the Amendment have been entered, and were sufficient to overcome the various claim objections. No amendments have been proposed after the final Office Action.

V. SUMMARY OF THE INVENTION

The Appellant's claimed invention will now be summarized with reference to the

corresponding parts of the Appellant's specification and drawings.

The present invention provides an image processing apparatus and method that enables a substantial reduction in power consumption as compared to the prior art. The invention provides, among other things, more efficient polygon rendering than the prior art. As explained on pages 1 to 4 of the specification, polygon rendering uses unit graphics, such as triangles, to express a three-dimensional model (page 1, line 22, through page 2, line 1). Processing is performed for interpolation of coordinates inside the unit graphic based on the values at the respective vertexes of the unit graphic (page 2, lines 2 to 8).

A problem with conventional polygon rendering techniques is that the processing is typically performed simultaneously (in parallel) for all of the pixels (e.g., 8 pixels) in a predetermined block, including the pixels outside the unit graphic (page 3, line 3, through page 4, line 10). The results of the processing operations for the pixels outside the unit graphic are invalid, thereby wasting resources and causing an unnecessary increase in power consumption (page 4, lines 11 to 18). Simply stated, the present invention solves this problem by stopping the operation of individual pixel processing circuits when it is determined that the corresponding pixel is outside the unit graphic, thereby conserving power (page 5, lines 4 to 16). As a result, a power source having a small and simple configuration can be used in the processing apparatus (page 34, lines 17 to 20).

The Appellant's invention, as recited in independent claim 1, provides an image processing apparatus 12, 13 comprising a plurality of pixel processing circuits 200_1-205_8 and a

control circuit 210_1-215_8 (page 21, lines 17 to 22; page 23, lines 8 to 13; Fig. 3). The pixel processing circuits 200_1-205_8 are each provided for processing each of a plurality of pixel data (e.g., Z, R, G, B, α, s, t, q) to be processed simultaneously, for processing a plurality of input pixel data in parallel (page 29, lines 5 to 20; Fig. 3). The control circuit 210_1-215_8, which can be a clock enabler, operates to stop the operation of at least one of the pixel processing circuits 200_1-205_8 when the processing of the pixel data to be processed in the pixel processing circuit is not needed (page 24, lines 16 to 22; page 25, lines 15 to 20; page 26, lines 17 to 21; page 27, lines 9 to 13; page 27, line 24, to page 28, line 2).

According to one embodiment, and as recited in independent claim 6, the image processing apparatus can be used for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape (i.e., polygon rendering). Pixel data of a plurality of pixels positioned within each graphic unit is processed on the basis of the same processing conditions. The result of the processed pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously is used as valid data in the image processing apparatus. The image processing apparatus includes a pixel position judging circuit 10 for judging whether or not a corresponding pixel is positioned within the graphic unit for each of the plurality of pixel data to be processed simultaneously (page 19, line 21, to page 20, line 1). The control circuit 210_1-215_8 is then used to stop the operation of the pixel processing circuits 200_1-205_8 other than the processing circuits for processing pixel data of pixels positioned within the graphic unit based on the judgement of

the pixel position judging circuit 10.

According to another embodiment of the invention, as recited in independent claims 11 and 16, the pixel processing circuits 405_1-405_8 (Figs. 5 and 6) are used for blending a plurality of first pixel data (R, G, B, α) with a plurality of second pixel data (R, G, B) stored in a display buffer 21 by blending ratios α indicated by a blending ratio data set for each pixel to produce third pixel data (page 38, line 23, to page 39, line 5). The control circuit 415_1-415_8 is then used to judge whether or not the pixel processing circuits 405_1-405_8 will perform the blending and to stop the operation of the pixel processing circuits 405_1-405_8 when judging that the blending will not be performed, such as when the α data is "0" or when the corresponding pixel is not positioned within the graphic unit (page 39, lines 6 to 18).

According to another embodiment of the invention, as recited in independent claims 17 and 21, the image processing apparatus includes a storage circuit (or z-buffer) 22 containing pixel depth data z, and the pixel data being processed by the pixel processing circuits 500_1-500_8 (Figs. 7 and 8) includes a plurality of first depth data z which is compared with the depth data z in the storage circuit 22 (page 42, lines 6 to 14). In this embodiment, the control circuit 510_1-510_8 judges whether or not to rewrite the pixel depth data z in the storage circuit 22 and stops operation of the corresponding pixel processing circuit 500_1-500_8 when judging not to rewrite or when the corresponding pixel is not positioned within the graphic unit (page 44, lines 9 to 14; page 45, lines 5 to 12; page 49, line 7, to page 50, line 5).

According to other aspects of the present invention, the clock enablers 210_1-215_8

of the pixel processing circuits 200_1-205_8 operate on the basis of a clock signal S225 (page 23, lines 8 to 13). The control circuit 10 supplies the pixel processing circuits 200_1-205_8 with the clock signal S225 when it is judged that the pixel processing or blending is needed, such as when the pixels are positioned inside the graphic unit to be processed. The control circuit 10 stops the supply of the clock signal S225 to the pixel processing circuits 200_1-201_8 when it is judged that the pixel processing or blending is not needed, such as when the pixels are not positioned inside the graphic unit to be processed.

According to other aspects of the present invention, the pixel processing circuits each comprises a plurality of processing circuits (e.g., 200_1 and 201_1 in Fig. 4) connected in series to form a pipeline circuit. Each of the plurality of processing circuits connected in series within the pixel processing circuit has a flag storage portion 224. The flag storage portions 224 of the plurality of processing circuits are connected in series to constitute a shift register. The shift register is used to control pipeline processing within the pixel processing circuit and the supply of the clock signal $S250_1$.

In summary, the main features and variations of the Appellant's invention provide an image processing apparatus having a reduced power consumption by selectively stopping the operation of pixel processing circuits when judging that the pixel processing is not needed (e.g., when the corresponding pixel is outside a graphic unit being processed or has a blending ratio α of 0). The prior art relied upon by the Examiner does not provide such a system.

VI. REFERENCES OF RECORD

The following references were relied upon by the Examiner in the final Office Action:

1. U.S. Patent No. 5,179,638 issued to Dawson et al. ("Dawson et al.");
2. Japanese Patent Publication No. 09130570 of Kiyoto ("Kiyoto");
3. U.S. Patent No. 5,977,987 issued to Duluk, Jr. ("Duluk, Jr."); and
4. U.S. Patent No. 5,742,796 issued to Huxley ("Huxley").

VII. ISSUES

The issues presented for consideration in this appeal are as follows:

1. Whether the Examiner erred in rejecting claims 1 to 3, 5 to 8, 10, 22 to 24 and 26 to 29 under 35 U.S.C. § 103(a) as being unpatentable over Dawson et al. in view of Kiyoto;

2. Whether the Examiner erred in rejecting claims 4, 9, 25 and 30 under 35 U.S.C. § 103(a) as being unpatentable over Dawson et al. in view of Kiyoto, and further in view of Duluk, Jr.;

3. Whether the Examiner erred in rejecting claims 11 to 13, 15 to 19, 21, 31 to 33, 35 to 38 and 40 under 35 U.S.C. § 103(a) as being unpatentable over Dawson et al. in view of Huxley and Kiyoto; and

4. Whether the Examiner erred in rejecting claims 14, 20, 34 and 39 under 35 U.S.C. § 103(a) as being unpatentable over Dawson et al. in view of Huxley and Kiyoto, and

further in view of Duluk, Jr.

VIII. GROUPING OF CLAIMS

It is respectfully submitted that the claims do not stand or fall together as a single group for purposes of this appeal. More specifically, it is submitted that the claims on appeal can be grouped into the following nine groups:

1. Claims 1 to 3, 5 to 8, 10, 22 to 24 and 26 to 29 stand or fall together;
2. Claims 4, 9, 25 and 30 stand or fall together;
3. Claims 11, 13, 15, 19, 31, 33, and 38 stand or fall together;
4. Claims 12 and 32 stand or fall together;
5. Claims 16 and 35 stand or fall together;
6. Claims 17 and 36 stand or fall together;
7. Claims 18 and 37 stand or fall together;
8. Claims 21 and 40 stand or fall together; and
9. Claims 14, 20, 34 and 39 stand or fall together.

The arguments set forth in the following section provide reasons why each of these groups should be considered separately.

IX. ARGUMENTS

A. The Examiner Erred in Rejecting Claims 1 to 3, 5 to 8, 10, 22 to 24 and 26 to 29 under 35 U.S.C. § 103(a) As Being Unpatentable over Dawson et al. in view of Kiyoto

Claims 1 to 3, 5 to 8, 10, 22 to 24 and 26 to 29 stand finally rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Kiyoto. The Examiner contends that Dawson et al. teaches an image processing apparatus having all of the features of the Appellant's claimed invention, except for a means for stopping the operation of the pixel processing circuits for pixels that do not lie within the graphic units. The Examiner relies upon Kiyoto for a teaching of this feature. This rejection is improper and should be reversed for the following reasons.

Dawson et al. discloses an image processing apparatus for providing a texture mapped perspective view for digital map systems. Dawson et al.'s system includes means for storing elevation data and texture data, means for scanning a projected view volume from the elevation data storing means, means for processing the projected view volume, means for generating a plurality of planar polygons, and means for rendering images.

The image processing system of Dawson et al. uses a rendering engine 34 that receives an input of coordinates for planar polygons from a tiling engine 40, and then generates image data across each polygon by interpolating color, depth, elevation, and transparency from pixels on the edges of the polygon (see column 8, lines 26 to 65). This is an image processing technique referred to as "polygon rendering," which is described in the Background section of the

Appellant's specification (see page 1, line 22, through page 2, line 8).

In conventional polygon rendering, such as that performed by the engine 34 of Dawson et al., processing is performed in parallel (simultaneously) for all pixels in a predetermined block. Since some of the pixels in a predetermined block fall outside the polygon being rendered and are not needed, the operations performed on these pixels become invalid. In imaging devices such as the device described by Dawson et al., processing is performed on all of the plurality of pixels located in a predetermined block regardless of whether they are inside the polygon or not. Thus, a large number of invalid operations are performed and power consumption is increased.

Kiyoto fails to remedy the deficiencies in the image processing system of Dawson et al. Kiyoto discloses an image forming device (e.g., a color copying machine) which includes a scanner, a printer, and an image processing means. The device includes an image processing means which receives and processes image data based on picture image clock signals for each processing block that receives image data from an external device, such as a scanner. A supply/inhibit signal is used to inhibit application of the image clock signal to processing blocks that do not receive image data. By stopping application of the image clock signal to processing blocks which are not in use, power consumption of the image forming device is reduced.

In the image processing device of Kiyoto, the image clock signal is inhibited for an entire processing block, and not just for selected pixels or pixel processing circuits within a processing block. This is a significant distinction between the Appellant's claimed invention and

the teachings of Kiyoto. If the teachings of Kiyoto could somehow be applied to image the polygon 30 shown in Fig. 12 of the Appellant's drawings, the rendering would be performed unconditionally on all of the pixels in the blocks 31, 32, and 33 because at least part of the pixels of each block 31, 32, 33 are within the polygon 30. As a result, a large number of invalid operations would occur and power consumption would be substantially higher than required by the Appellant's invention.

Moreover, Kiyoto does not teach an image processing device for use with "polygon rendering." The image processing device of Kiyoto was apparently developed for color copying machines and the like, and not for three-dimensional computer graphics and the like which use polygon rendering techniques. There is no teaching or suggestion in Kiyoto of stopping an image clock signal to selected pixel processing circuits of a plurality of pixels to be processed simultaneously (i.e., within a processing block), nor of stopping an image clock signal to a selected pixel processing circuit based on a judgment that the corresponding pixel is positioned outside a graphic unit to be processed.

It would not have been obvious to modify the image processing device of Dawson et al. based on the teachings of Kiyoto to arrive at the Appellant's claimed invention. As explained above, there is no teaching in either of these applied references of an image processing device having a means for stopping operation of selected pixel processing circuits within a group of such circuits to be operated simultaneously when it is determined that processing of the corresponding pixel data is not needed (e.g., when the corresponding pixel is positioned outside

the graphic unit to be processed). While Dawson et al. teaches image processing using polygon rendering methods, it is only representative of the related art image processing techniques described by the Appellant on pages 1 to 4 of the specification. On the other hand, the disclosure of Kiyoto does not even relate to imaging devices that use polygon rendering methods, and therefore has little relevance to the Appellant's claimed invention.

For these reasons, it is respectfully submitted that Kiyoto provides no suggestion or motivation for modifying the image processing apparatus of Dawson et al. in the manner proposed by the Examiner. The mere fact that two references can be combined or modified does not render the resultant combination obvious under 35 U.S.C. 103 unless the prior art also teaches or suggests the desirability of the combination. In re Mills, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990) (although a prior art device "may be capable of being modified," there must be a suggestion or motivation in the reference to do so"); see, also, M.P.E.P. § 2143.01 (8th ed.).

The Examiner contends on page 13, last paragraph, of the final Office Action that the rejected claims do not recite the features upon which the Appellant relies in traversing the rejection. The Appellant respectfully disagrees. The arguments set forth above distinguish the claims on appeal from the cited references of Dawson et al. and Kiyoto using limitations found in the claims. These limitations, including for example, the claimed "control circuit for stopping the operation of at least one of said pixel processing circuits when the processing ... is not needed" recited in independent claim 1, and the claimed "control circuit for stopping the

operation of the pixel processing circuits ... on the basis of the results of the judgement of said pixel position judging circuit" recited in independent claim 6, are not found in the cited references. Similar limitations are recited in the Appellant's independent method claims 22 and 27, which also are not found in the cited references.

To establish *prima facie* obviousness of a claimed invention under 35 U.S.C. 103, all of the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); see, also, M.P.E.P. §2143.03 (8th ed.). Since the above-mentioned limitations in independent claims 1, 6, 22 and 27 are neither taught nor suggested by the applied references, it is respectfully submitted that the Examiner has failed to establish a *prima facie* case of obviousness for the invention of these claims.

Accordingly, the Appellant respectfully submits that the claimed invention of claims 1 to 3, 5 to 8, 10, 22 to 24, and 26 to 29 would not have been obvious to one of ordinary skill in the art from the combined teachings of Dawson et al. and Kiyoto.

B. The Examiner Erred in Rejecting Claims 4, 9, 25 and 30 under 35 U.S.C. § 103(a) As Being Unpatentable over Dawson et al. in View of Kiyoto, and Further in View of Duluk, Jr.

Claims 4, 9, 25 and 30 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Kiyoto, as applied to claim 27, and further in view of Duluk, Jr. (U.S. Patent No. 5,977,987). The Examiner relies upon Duluk, Jr. for a teaching of connecting a flag storage portion to a shift register in series to control pipeline processing. This

rejection is improper and should be reversed for the following reasons.

Claims 4, 9, 25 and 30 are dependent, directly or indirectly, on independent claims 1, 6, 22 and 27, respectively. Therefore, it is respectfully submitted that these claims are allowable over the cited references for at least the same reasons explained above concerning independent claims 1, 6, 22 and 27. It is further noted that the image processing system disclosed by Duluk, Jr. does not have a means for stopping operation of selected pixel processing circuits within a group of pixels to be processed simultaneously based on a judgment that the corresponding pixel is positioned outside the graphic unit to be processed or is otherwise not needed. Thus, Duluk, Jr. fails to remedy the deficiencies in the combined teachings of Dawson et al. and Kiyoto, as explained above.

Accordingly, the Appellant respectfully submits that the claimed invention of claims 4, 9, 25 and 30 would not have been obvious to one of ordinary skill in the art from the combined teachings of Dawson et al., Kiyoto and Duluk, Jr.

C. The Examiner Erred in Rejecting Claims 11 to 13, 15 to 19, 21, 31 to 33, 35 to 38 and 40 under 35 U.S.C. § 103(a) As Being Unpatentable over Dawson et al. in View of Huxley and Kiyoto

Claims 11 to 13, 15 to 19, 21, 31 to 33, 35 to 38 and 40 stand finally rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Huxley and Kiyoto. This rejection is improper and should be reversed for the following reasons.

Claims 11 and 31

Independent claims 11 and 31 recite an image processing apparatus and method, respectively, which use a plurality of pixel processing circuits to simultaneously blend a plurality of first and second pixel data based on a blending ratio data set for each pixel; judge based on the blending ratio data whether to perform the blending by pixel processing circuits; and stop the operation of the corresponding pixel circuits when judging that they will not perform the blending. The cited references fail to teach these features of the Appellant's invention.

The image processing method disclosed by Dawson et al. is described above. As noted by the Examiner, Dawson et al. fails to teach the use of blending ratio data in pixel processing. While Huxley does teach the use of blending ratio data in pixel processing, Huxley does not teach or suggest a control circuit or process step that judges whether or not the pixel processing circuits will perform blending, and then stops the operation of respective pixel processing circuits in which blending will not be performed.

Huxley discloses an image processing method having an alpha blend unit which blends the source color and the destination color according to an alpha blend equation to produce an output color (see column 61, lines 5 to 67). As noted by the Examiner, Huxley also mentions the use of a NoAlphaBuffer bit in the AlphaBlendMode message when no alpha buffer is present. However, Huxley does not teach a system or method in which a determination is made whether alpha blending will be performed by the pixel processing circuits, nor in which the pixel processing circuits that will not perform alpha blending are stopped based on such a determination. Instead, it appears that the pixel processing circuits in Huxley continue

processing the data unless the alpha blend mode is completely disabled (column 61, lines 65 to 67).

Claims 12 and 32

Claims 12 and 32, which depend upon claims 11 and 31, respectively, are allowable over the cited references for the following additional reasons. Claims 12 and 32 recite an image processing apparatus and method, respectively, in which the supply of clock signal to a pixel processing circuit is stopped when it is judged that the circuit will not perform blending of the first and second pixel data.

Huxley does not teach or suggest a system in which a clock signal is stopped to stop the operation of a pixel processing circuit after determining that it will not perform alpha blending. In fact, Huxley appears to teach away from such a system in column 7, lines 11 to 15, by stating that messages should continue to be passed on to other units even after determining a pixel is not going to be updated.

The Examiner contends on page 14 of the final Office Action that the pixel processing circuits of Huxley would still need to process other attributes associated with the pixel in subsequent clock cycles. This statement by the Examiner is inconsistent with the language of the Appellant's claim 12 which recites, among other things, that the control circuit "stops the supply of said clock signal to said pixel processing circuit when judging that it will not perform said blending." A similar limitation is found in method claim 32. These limitations are not found in the teachings of Huxley.

Similarly, the combined teachings of Dawson et al. and Kiyoto lack any teaching or suggestion of an image processing system in which clock signals for individual pixel processing circuits in a block of such circuits to be processed simultaneously are selectively stopped based on a judgment that blending or other processing is not required of such pixel processing circuit.

Claims 16 and 35

Independent claims 16 and 35 recite an image processing apparatus and method, respectively, in which an image is expressed as a composite of graphic units of predetermined shape, a plurality of pixel processing circuits are used to blend a plurality of first and second pixel data based on a blending ratio data set, a control circuit judges whether or not a pixel is positioned within a graphic unit to be processed for each of the pixels being simultaneously processed, and the control circuit stops the operation of pixel processing circuits for pixels outside of the graphic units or those in which it is determined that blending will not be performed.

Claims 16 and 35 are allowable over the cited references for generally the same reasons explained above regarding these cited references. Specifically, none of the cited references teach stopping the operation of pixel processing circuits that are judged to lie outside of the graphic unit to be processed, as in the Appellant's invention. As explained above, Kiyoto fails to teach this feature of the claimed invention because in Kiyoto, the image clock signal is stopped for an entire processing block, and not for selected processing circuits within the

processing block. Moreover, the teachings of Kiyoto are directed to color copiers, scanners and the like and have little relevance to the three-dimensional image processing technology of the Dawson et al. and Huxley references.

Claims 17 and 36

Independent claims 17 and 36 recite an image processing apparatus and method, respectively, in which a plurality of pixel processing circuits are used to produce a plurality of second pixel data from a plurality of first pixel data, first depth data of the first pixel data is compared with second depth data of a plurality of third data stored in a storage circuit, and a control circuit judges whether or not to rewrite the third pixel data by the second pixel data and stops the operation of the corresponding pixel circuits when judging that they will not perform the rewrite.

The image processing systems disclosed by each of the cited references is described above. As noted by the Examiner, Dawson et al. fails to teach depth comparison between pixel data. While Huxley does teach the use of depth comparison between pixel data, Huxley does not teach or suggest the claimed circuit control recited in claims 17 and 36. Specifically, Huxley does not disclose a process step that judges whether or not to rewrite the depth data stored in the storage circuit by the first depth data, and then stops the operation of respective pixel processing circuits in which the depth data will not be rewritten. As explained above, Huxley appears to teach away from such a system in column 7, lines 11 to 15, by stating that messages should continue to be passed on to other units even after determining a pixel is not

going to be updated.

Claims 18 and 37

Claims 18 and 37, which depend upon claims 17 and 36, respectively, are allowable over the cited references for the following additional reasons. Claims 18 and 37 recite an image processing apparatus and method, respectively, in which the supply of clock signal to a pixel processing circuit is stopped when it is judged that the circuit will not perform a rewrite of depth data stored in a storage circuit for a corresponding pixel.

As explained above, Huxley does not teach or suggest a system in which a clock signal is stopped to stop the operation of a pixel processing circuit after determining that it will not perform a rewrite of depth data in a storage circuit. Similarly, the combined teachings of Dawson et al. and Kiyoto lack any teaching or suggestion of an image processing system in which clock signals for individual pixel processing circuits in a block of such circuits to be processed simultaneously are selectively stopped based on a judgment that a certain operation (i.e., depth data rewrite) is not required of such pixel processing circuit.

Claims 21 and 40

Independent claims 21 and 40 are allowable for at least the same reasons explained above in connection with the Examiner's rejections of independent claims 6, 17, 27 and 36, which separately recite similar features of the Appellant's invention.

Accordingly, the Appellant respectfully submits that the claimed invention of claims 11 to 13, 15 to 19, 21, 31 to 33, 35 to 38 and 40 would not have been obvious to one of

ordinary skill in the art from the combined teachings of Dawson et al., Kiyoto and Duluk, Jr.

D. The Examiner Erred in Rejecting Claims 14, 20, 34 and 39 under 35 U.S.C. § 103(a) As Being Unpatentable over Dawson et al. in View of Huxley and Kiyoto, and further in view of Duluk, Jr.

Claims 14, 20, 34 and 39 stand finally rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Huxley and Kiyoto, and further in view of Duluk, Jr. The Examiner relies upon Duluk, Jr. for a teaching of a flag storage portion connected to the shift register in series. This rejection is improper and should be reversed for the following reasons.

Claims 14, 20, 34 and 39 are dependent, directly or indirectly, on independent claims 11, 17, 31 and 36, respectively. Therefore, it is respectfully submitted that these claims are allowable over the cited references for at least the same reasons explained above concerning these independent claims. It is further submitted that the image processing system disclosed by Duluk, Jr. fails to remedy the various deficiencies in the combined teachings of Dawson et al., Huxley and Kiyoto, as explained above.

X. CONCLUSION

In view of the foregoing, it is respectfully submitted that the final rejections of claims 1 to 40 are improper and should not be sustained. Therefore, a reversal of the final rejections of the Examiner is respectfully requested.

Respectfully submitted,

Dated: **May 28, 2002**

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

1. An image processing apparatus comprising:

a plurality of pixel processing circuits, each provided for processing each of a plurality of pixel data to be processed simultaneously, for processing a plurality of input pixel data in parallel; and

a control circuit for stopping the operation of at least one of said pixel processing circuits when the processing of said pixel data to be processed in the pixel processing circuit is not needed.

2. An image processing apparatus as set forth in claim 1, wherein:

said pixel processing circuits operate on the basis of a clock signal; and

said control circuit supplies said pixel processing circuits with said clock signal when judging the pixel processing is needed and stops the supply of said clock signal to said at least one of said pixel processing circuits when judging the pixel processing is not needed.

3. An image processing apparatus as set forth in claim 2, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series to form a pipeline circuit.

4. An image processing apparatus as set forth in claim 3, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control pipeline processing within the pixel processing circuit and the supply of said clock signal.

5. An image processing apparatus as set forth in claim 1, wherein each of said pixel processing circuits performs processing with respect to pixel data of red (R), green (G), and blue (B) of a pixel.

6. An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a pixel position judging circuit for judging whether or not a corresponding pixel is positioned within said graphic unit for each of the plurality of pixel data to be processed simultaneously;

a plurality of pixel processing circuits for processing a plurality of pixel data to be processed simultaneously mutually in parallel; and

a control circuit for stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among said plurality of pixel processing circuits on the basis of the results of the judgement of said pixel position judging circuit.

7. An image processing apparatus as set forth in claim 6, wherein:

each of said pixel processing circuits operates on the basis of a clock signal; and

said control circuit supplies said clock signal to pixel processing circuits processing the pixel data of pixels positioned inside the graphic unit to be processed, and stops the supply of said clock signal to pixel processing circuits processing the pixel data of pixels not positioned inside the graphic unit to be processed.

8. An image processing apparatus as set forth in claim 7, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series so as to perform pipeline processing.

9. An image processing apparatus as set forth in claim 8, wherein each of said plurality of processing circuits connected in series within each said pixel processing

circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

10. An image processing apparatus as set forth in claim 6, wherein:

said pixel position judging circuit adds validity data indicating the result of the judgement to pixel data processed by said pixel processing circuits; and

said control circuit judges based on the validity data whether to stop the operation of said pixel processing circuits.

11. An image processing apparatus comprising:

a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, for blending a plurality of first pixel data and a corresponding plurality of second pixel data by blending ratios indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data; and

a control circuit for judging whether or not said pixel processing circuits will perform said blending and stopping the operation of said pixel processing circuits when judging that said blending will not be performed.

12. An image processing apparatus as set forth in claim 11, wherein:

each of said pixel processing circuits operates on the basis of a clock signal; and

said control circuit supplies each respective pixel processing circuit with said clock signal when judging that said pixel processing circuit will perform blending and stops the supply of said clock signal to said pixel processing circuit when judging that it will not perform said blending.

13. An image processing apparatus as set forth in claim 12, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series so as to perform pipeline processing.

14. An image processing apparatus as set forth in claim 13, wherein each of said plurality of processing circuits connected in series within each said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

15. An image processing apparatus as set forth in claim 11,

further comprising a storage circuit for storing said second pixel data, wherein

said control circuit rewrites the second pixel data stored in said storage circuit by said first pixel data when judging that blending will not be performed and

rewrites the second pixel data stored in the storage circuit by said third pixel data when judging that blending will be performed.

16. An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a plurality of image processing circuits, provided for a plurality of pixels to be processed simultaneously, for blending a plurality of first pixel data and a corresponding plurality of second pixel data by a blending ratio indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data; and

a control circuit for judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously and stopping the operation of a pixel processing circuit when judging that said corresponding pixel is not positioned within said graphic unit or when judging that said blending will not be performed on the basis of said blending ratio data.

17. An image processing apparatus comprising:

a storage circuit;

a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, for producing a plurality of second pixel data from a plurality of first pixel data;

a comparing circuit for comparing a plurality of first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in said storage circuit in correspondence with said plurality of first depth data; and

a control circuit for judging whether or not to rewrite third pixel data corresponding to second depth data stored in said storage circuit by second pixel data and stopping the operation of the corresponding pixel processing circuit when judging not to rewrite.

18. An image processing apparatus as set forth in claim 17, wherein:

said pixel processing circuit operates on the basis of a clock signal; and

said control circuit supplies said pixel processing circuit with said clock signal when judging to rewrite the third pixel data stored in the storage circuit with the second pixel data and stopping the supply of said clock signal to the pixel processing circuit when judging not to rewrite the third pixel data stored in the storage circuit by the second pixel data.

19. An image processing apparatus as set forth in claim 18, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series so as to perform pipeline processing.

20. An image processing apparatus as set forth in claim 19, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

21. An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a storage circuit;

a plurality of pixel processing circuits, provided for a plurality of pixels to be

processed simultaneously, for producing a plurality of second pixel data from a plurality of first pixel data;

a comparing circuit for comparing a plurality of first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in said storage circuit in correspondence with said plurality of first depth data; and

a control circuit for judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously, judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison, and stopping the operation of at least one of said pixel processing circuits when judging that the corresponding pixel is not positioned within said graphic unit or when judging not to rewrite.

22. An image processing method for performing image processing by using pixel processing circuits, each provided for each of a plurality of pixels to be processed simultaneously, for processing a plurality of input pixel data in parallel, comprising the steps of:

judging whether or not on the basis of said pixel data the pixel processing of said processing circuits is needed; and

stopping operation of at least one of said pixel processing circuits when judging

the pixel processing of said at least one processing circuit is not needed.

23. An image processing method as set forth in claim 22, further comprising the steps of:

supplying said pixel processing circuit with a clock signal when judging the pixel processing is needed; and

stopping the supply of said clock signal to said pixel processing circuit when judging the pixel processing is not needed.

24. An image processing method as set forth in claim 23, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

25. An image processing method as set forth in claim 24, wherein each of said plurality of processing circuits connected in series within each of said pixel processing circuits has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

26. An image processing method as set forth in claim 22, wherein said pixel

processing is processing with respect to pixel data for deciding output of red (R), green (G), and blue (B) of a pixel.

27. An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of the plurality of pixel data to be processed simultaneously;

processing a plurality of pixel data to be processed simultaneously mutually in parallel in a plurality of pixel processing circuits; and

stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among said plurality of pixel processing circuits on the basis of the results of the judgement.

28. An image processing method as set forth in claim 27, further comprising the

steps of:

supplying a clock signal to the pixel processing circuits processing the pixel data of pixels positioned inside the graphic unit to be processed; and

stopping the supply of said clock signal to pixel processing circuits processing the pixel data of pixels not positioned inside the graphic unit to be processed.

29. An image processing method as set forth in claim 28, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

30. An image processing method as set forth in claim 29, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

31. An image processing method comprising the steps of:

using a plurality of pixel processing circuits provided for a plurality of pixels to be processed simultaneously to blend a plurality of first pixel data and a plurality of second pixel data by blending ratios indicated by a blending ratio data set for each pixel to

produce a plurality of third pixel data;

judging based on said blending ratio data whether to perform said blending by said pixel processing circuits; and

stopping the operation of at least one of said pixel processing circuits when judging that said at least one pixel processing circuit will not perform said blending.

32. An image processing method as set forth in claim 31, further comprising the steps of:

supplying a corresponding pixel processing circuit with a clock signal when judging that said corresponding pixel processing circuit will perform blending; and

stopping the supply of said clock signal to at least one of said pixel processing circuits when judging that said at least one pixel processing circuit will not perform said blending.

33. An image processing method as set forth in claim 32, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

34. An image processing method as set forth in claim 33, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has

a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

35. An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

using a plurality of image processing circuits, provided for a plurality of pixels to be processed simultaneously, to blend a plurality of first pixel data and a plurality of second pixel data by a blending ratio indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data;

judging whether or not a corresponding pixel is positioned within a corresponding one of said graphic units for each of said plurality of pixels to be processed simultaneously; and

stopping the operation of at least one of said pixel processing circuits when judging that the corresponding pixel is not positioned within said graphic unit to be

processed or when judging that said blending will not be performed on the basis of said blending ratio data.

36. An image processing method comprising the steps of:

using a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data;

comparing a plurality of first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in a storage circuit in correspondence with said plurality of first depth data; and

judging whether or not to rewrite third pixel data corresponding to second depth data stored in said storage circuit by second pixel data and stopping the operation of the corresponding pixel processing circuit when judging not to rewrite.

37. An image processing method as set forth in claim 36, further comprising the steps of:

supplying said pixel processing circuit with a clock signal when judging to rewrite the third pixel data stored in the storage circuit with the second pixel data; and

stopping the supply of said clock signal to the pixel processing circuit when judging not to rewrite the third pixel data stored in the storage circuit by the second pixel

data.

38. An image processing method as set forth in claim 37, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

39. An image processing method as set forth in claim 38, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

40. An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

using a plurality of pixel processing circuits, provided for a plurality of pixels to

be processed simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data;

comparing a plurality of said first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in a storage circuit in correspondence with said plurality of first depth data;

judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously, judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison; and

stopping the operation of at least one of said pixel processing circuits when judging that the corresponding pixel is not positioned within said graphic unit to be processed or when judging not to rewrite.